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4H-SiC Self-Aligned Implant-Diffused Structure for Power DMOSFETs

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Abstract

In this paper we report the first self-aligned vertical implant-diffused (VID) and lateral implant – diffused (LID) MOSFET test structures in 4H-SiC by using the differing diffusivities of implanted boron and nitrogen in silicon carbide. Boron diffusion was studied with and without nitrogen co-implants. The optimal diffusion conditions resulted in a 1 μm lateral diffusion width. A blocking voltage of 300 V was achieved in these test structures with a blocking layer thickness of only about 2 μm.

Introduction

Because of the high performance, reliability of design, and the relative ease in fabrication obtained by using diffusion to form a self-aligned gate, the self-aligned DMOS structure is the most common power MOSFET design produced in the Si industry. The reason this structure has classically not been considered for SiC MOSFETs was because of the extreme temperatures required for obtaining significant dopant diffusion in SiC. At these temperatures, severe degradation of the SiC surface can occur, resulting in step bunching and silicon evaporation.

All SiC DMOSFETs reported to date have utilized a double implanted MOS (DIMOS) [1-3] structure instead of the conventional, less expensive, diffused MOS (DMOS) structure with a self-aligned channel. The DIMOS structure requires separate implant masks for the formation of the source and channel regions. In addition, these devices have demonstrated relatively low channel mobility, a possibly due to damage imparted to the channel by the implantation process. Unlike Si, it is difficult to fully remove this implant damage in SiC. This damage can degrade the mobility severely through the implanted regions.

Thus, a diffused DMOSFET should have substantial fabrication and performance advantages over the DIMOS device. The first step in pursuing such a device is to understand and control the dopant diffusion. Boron was chosen as the dopant species because it acts as a p-type dopant in SiC, and diffuses more easily than Al, the other common p-type dopant in SiC.

Dopant Diffusion

The diffusivity of implanted boron and nitrogen in 4H-SiC at different implantation conditions (same depth of B and N; B deeper then N; B shallower then N; different order and temperature during implants) and annealing conditions (temperature range of 1500 – 1700°C for 5 - 30 minutes) was measured via SIMS. The most relevant profiles are shown in Figs. 1 and 2.

Fig. 1a. shows the diffusion in the "tail" region of the implanted B (90 keV, 2.0×10^{14} cm^{-2}) during a 1700°C anneal for 30 minutes. The boron diffused in this region at anneal temperatures in excess of 1500°C, and did not vary significantly for anneal temperatures between 1500°C and 1700°C. It was found that boron diffuses during the first few minutes of the anneal with an effective diffusion coefficient of 2×10^{-12} cm^2/sec, and then is fairly stable.

The same boron diffusivity was observed in this "tail" region when the B (90 keV, 2.0×10^{14} cm^{-2}) was co-implanted with N (150 keV, 1.8×10^{14} cm^{-2}). However, the boron diffusion concentration starts at 1×10^{17} cm^{-3}, instead of the 1×10^{18} cm^{-3} observed without the co-implants. This implies

that nitrogen co-implants can be used for control of the boron diffusivity in the "tail" region.

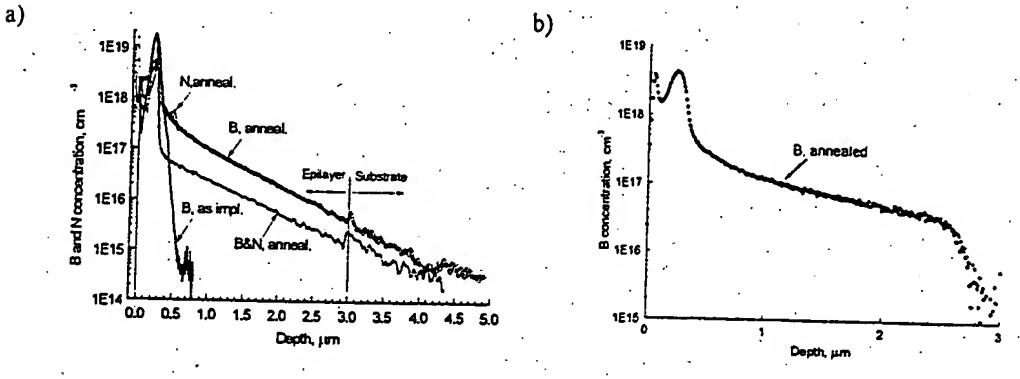

Figure 1. SIMS data for B implants into 4H-SiC before and after annealing at 1700°C for 30 minutes. a) with and without N co-implants along the (0001) axis; b) along the (11$\bar{2}$0) axis.

Fig. 1b demonstrates that the diffusion of implanted B (90 keV, 2.0×10^{14} cm^{-2}) depends on the crystal orientation. Diffusion along the (11$\bar{2}$0) axis is lower than in the (0001) axis. For the DMOSFET, diffusion in the lateral direction will be along the (11$\bar{2}$0) and (1$\bar{1}$00) axes. This lateral diffusion does not demonstrate the long tail observed in the vertical diffusion.

Diffusion of boron towards the surface is important for two reasons: 1) the boron can evaporate from the surface, dramatically reducing the amount available for diffusion into the channel region, which would be the lateral direction of a DMOSFET and 2) the boron can compensate the co-implanted nitrogen, increasing the source resistance.

Fig. 2 shows the B diffusion in the near-surface region. Fig. 2a illustrates the effect of anneal temperature on the boron distribution using 1500, 1600, and 1700°C anneals for 10 minutes. These samples were implanted at room temperature (RT) by B^+ (180 keV, 4×10^{15} cm^{-2}) and co-implanted with N^+ (25 keV, 1.5×10^{14} cm^{-2} and 60 keV, 2.5×10^{14} cm^{-2}). As shown on Fig.2a, implanting N^+ after B^+ reduces the evaporation of boron through the surface during anneals up to 1600°C. At 1700°C, the B significantly diffuses towards the surface.

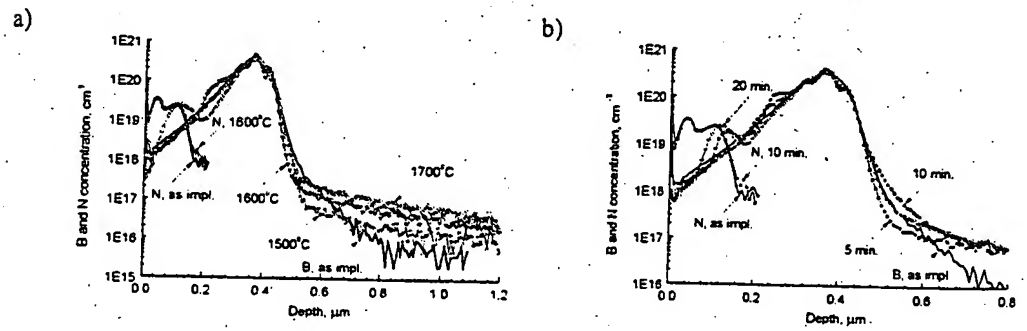

Fig. 2. B and N distributions as measured via SIMS after annealing at a) at 1500°C, 1600°C, or 1700°C for 10 minutes and b) at 1600°C for 5, 10 or 20 minutes.

In Fig. 2b, the B does not diffuse towards the surface during the 1600°C anneal for 5 or 10 minutes, but does during the 20 minute anneal. Although not illustrated in these figures, B annealed without the N co-implants diffuses towards the surface with a concentration level of about 1×10^{19} cm^{-2} and evaporates.

The diffusion of nitrogen in SiC was negligible and can be used as a reference for identifying etching or growing processes during an anneal. As reported by T. Troffer et. al. [5], a boron peak within 40 nm of the surface was measured. However, this peak can be the result of a growing process during an anneal in the prescense of SiC vapor, as identified by using the N peak as a

reference or "marker" as shown on Fig. 1a near the surface.

DMOS Device

DMOS test structures and FETs were fabricated with 3 μm thick epilayers (N_d-N_a= 2.2E15 cm^{-3}) on n-type substrates (N_d-N_a= 3E18 cm^{-3}) by using B^+ (180 keV, 4E15 cm^{-2}) and N^+ (25 and 60 keV with 1.5 and 2.5E14 cm^{-2}, respectively) implants into the same well at room temperature and anneals in the temperature range of 1500 – 1700 °C for 5 - 30 minutes. The cross section and top view of the DMOSFET are shown in Figure 2. The source-drain spacing varied from 0.5 to 30 μm. The gate oxide was 25 nm thick.

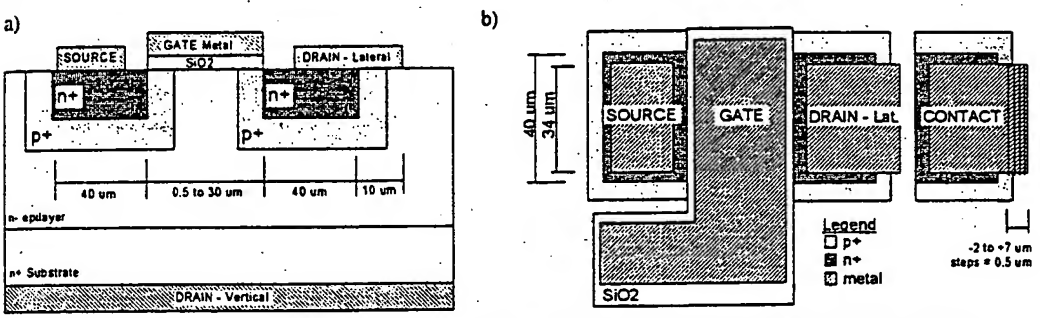

Fig.3. a.) Cross-sectional and b.) top-view of the test structure design for a vertical and lateral 4H-SiC n-channel implant diffused DMOSFET.

An example of one of the designs for this DMOSFET test structure is shown in Fig. 3, in both a cross-sectional and planar-view, with some of the critical dimensions. Two different structures for two different measurement techniques were designed in order to accurately determine the lateral boron diffusion distance. The first design consisted of a combined vertical and lateral MOSFET structure. Referring to Fig. 3, the first test structure consists of the Source, Gate, Drain-Lat (lateral) and Drain-Vert (vertical) regions. By incrementally narrowing the Source-to-Drain_Lat spacing, the test structure is transformed from a vertical MOSFET to a lateral MOSFET. Initially, with a Source-Drain_Lat spacing of 30 μm, the Source and Drain_Vert nodes act as the source and drain, respectively, of a vertical MOSFET. The diffused p-type boron region acts as the channel of the n-channel MOSFET.

As the Drain_Lat region is moved closer to the Source region, at some point the two p-type boron regions merge, creating a channel between the Source and the Drain_Lat regions; hence a lateral MOSFET device. As shown in the figure, the Drain_Lat contact overlaps the n^+ and p^+ regions of the drain, creating a substrate tie-down for the lateral device. By characterizing the 4-terminal device (3 top + bottom) and noting at which Source-Drain_Lat spacing the transition was made from a vertical to a lateral MOSFET, the boron diffusion distance could be determined. The maximum spacing was 30 μm and the minimum was 0.5 μm, with 0.1 increments in between these values for each reticle.

The second method for verifying the boron diffusion distance can be seen in Fig. 3b. A 2-terminal device is formed between the n-type region (labeled Contact) and the Drain_Vert region. The contact is incrementally stretched from the n-type nitrogen region, across the p-type boron region, and eventually to the n- epilayer. Initially, the Contact is fully enclosed by the n-type nitrogen region, creating an NPN transistor where the n-type nitrogen implant is the emitter, the diffused p-type boron region is the floating base, and the n-epilayer is the collector. Because there are back-to-back diodes, no current can be measured vertically through the chip. As the edge of the contact is stretched across the nitrogen-boron junction, the emitter and base regions are shorted together, yielding a diode between Contact and Drain_Vert, and the pn junction I-V characteristics can be observed. Finally, as the edge of the contact is stretched past the diffused boron region, the emitter, base and collector of the NPN device are shorted together, creating a resistive short between Contact and Drain_Vert. By characterizing the 2-terminal device and noting at which contact-overlap spacing the transition was made from a diode to a resistor, the boron diffusion distance could be determined.

The channel length was determined to be about 1.0 μm (thus the lateral boron diffusion length in excess of nitrogen diffusion was about 1.0 μm). The annealing condition that yielded this result was

the 1600 °C, 10 minute anneal. Other annealing conditions resulted in less diffusion or lower activation of boron in the channel region. The 1 μm lateral diffusion of the implanted B was in agreement with the distances measured on test samples with SIMS.

The DMOSFETs had a p-type channel surface concentration of about 2.5×10^{18} cm^{-3}, determinec by the relatively high threshold voltage of V_G = +6V and the gate oxide thickness of 25 nm. Figure 4a demonstrates the standard MOSFET characteristics that were observed, with excellent current saturation, indicating that there were no short-channel effects. The on-current at V_G = +18 V was

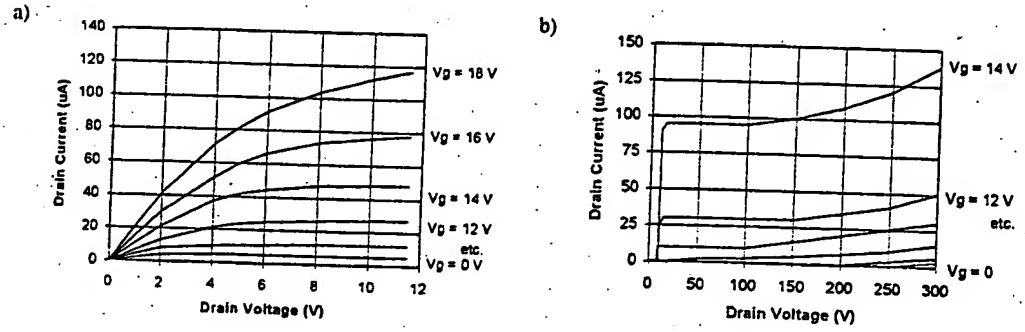

Fig.4. I-V characteristics of self-aligned 4H-SiC DMOS test structures produced by room temperature B^+ and N^- implantation and annealed at 1600°C for 10 minutes at a) low drain voltage and b) high drain voltage, showing 300 V blocking voltage for an approximate blocking layer thickness of <2μm (W = 80 μm, L_G = 1 μm).

about 1.5 mA/mm of gate periphery. The channel mobility derived from the I-V characteristics and the gate length that was measured for this diffused 4H-SiC vertical test structure was μ_n = 0.6 cm^2/V-sec, at a gate bias of 18 V (12 V above the threshold voltage). The best channel mobility in lateral DMOS structure was μ_n = 1.5 cm^2/V-sec. This value is quite low, but is not a typical for lateral MOSFETs in 4H-SiC. It has been proposed that the very low channel mobilities in 4H-SiC are due to a high density of interface states near the conduction band [4,6].

The highest blocking voltage achieved on these devices was 300 V, as shown in Figure 4b. This is despite the fact that the n^- blocking layer, after the boron was diffused, was probably less than 2 μm thick, and there was no high voltage edge termination on these devices.

Conclusions

The gate control and excellent blocking voltage of these DMOSFETs demonstrate for the first time that a DMOS technology in SiC may be a viable alternative to the DIMOS and UMOS structures. The feasibility has been demonstrated for developing a self-aligned DMOS technology in SiC that can achieve high voltage operation with greatly reduced fabrication costs. However, the low channel mobilities for these 4H-SiC devices indicates that further research is needed.

Acknowledgements

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